Service Manual

MP MASTER
MA29259

Digital Level and Noise Measuring Set PMD-1

for measuring telephone and sound-programme transmission circuits as well as wideband level measurements in the frequency range 20 Hz to 200 kHz

DIGITAL LEVEL AND NOISE MEASURING SET PMD-1

Service Manual 618 B...

1.11.77 Ü
0.2. 11.77 2428

Subject to change without notice
Printed in the Federal Republic of Germany

Wandel & Goltermann

PRECISION ELECTRONIC
MEASURING INSTRUMENTS

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6. PRELIMINARY REMARKS TO SERVICE MANUAL

6. PRELIMINARY COMMENTS TO THE SERVICING INSTRUCTIONS

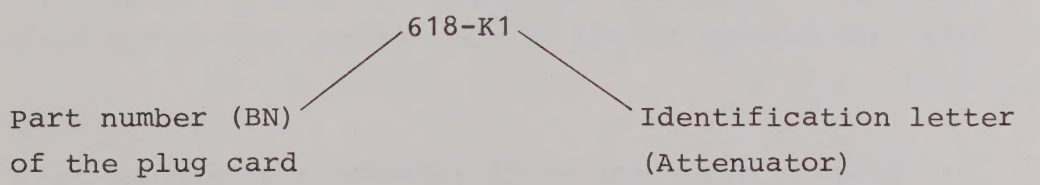
Section 6.1 to 6.3 explain the meanings of the abbreviations, symbols, and codes which are used in Chapters 7 to 10 and in the Appendix. Section 6.4 contains instructions for the test equipment, Section 6.5 for ordering spare parts.

6.1 Stripping and replacing the plug-in units

In order to carry out the servicing work on the power supply, the wiring board, and the modules (printed circuit board) of the unit, the four mounting screws on the rear wall of the unit must be loosened. The side walls and the base plate can now be removed.

The plug-in boards are equipped with high quality gold contacts in order to guarantee low contact resistances. In order to prevent undue wear on the contacts, the plug-in boards should not be replaced too often; they may be removed and inserted only with the mains plug removed from the supply.

The various printed circuit boards are identified in accordance with the following plan, e.g.:



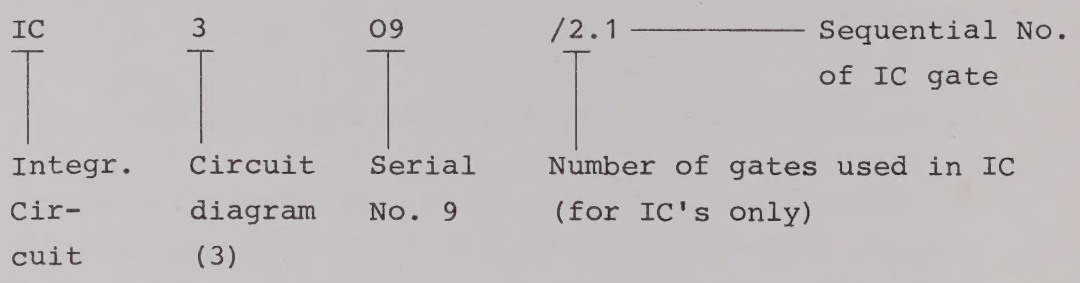
6.2 Component code

The modules and the circuit diagrams in the Appendix are identified by individual numbers, e.g.:

Converter ③

The position numbers of all circuit components in this

module start with the number 3. The two following digits number the components sequentially, e.g. 26 for capacitor C 326 or 17 for resistor R 317. The preceding letters define the type of component, and these are summarized in Section 6.4.



6.3 Internal connections

The connection pins of the plug strips (1b), (2) ... (7), (8c), (9a) ... (9c) are identified with a number of an upper case letter around the edge of the circuit diagrams (dotted and dashed line). The pins are also marked with the signal name. This refers to the digital low state (L) or to the digital high state (H) in the case of inverted signals.

The plug strips of the boards correspond to the socket strips whose arrangement is shown in the Appendix. The various contacts are accessible at this point and at the appropriate points of the adapter board (See Section 7.2).

In order to determine which internal connections lead from one board to another within the unit, or which signal has certain functions in a further circuit, the socket (strip) assignment lists in the Appendix are used. In these lists, the letters A to Z refer to the contacts on the component side and the numbers 1 to 22 refer to the contacts on the conductor side.

Examples on the basis of the socket (strip) assignment PMD-1, strip ⑤ (= signals on board ⑤ control).

1) Pin U with signal "Release converter" on strip (5) is connected to (7) 16, (4) U, and (3) U, i.e. to strip (7), contact 16, and to contact U on strips (4) and (3).

   The number 4 in column 1 means that a total of 4 branches leave contact U within the test area of the (company internal) automatic testing equipment, the number 39 designates the sequential test point number for the automatic card bed tester.

2) The signal "Current in" at strip (5), contact 7, is fed to strip (3), contact V and to contact 7 of strips (6) and (7).

6.4 Test equipment

The test equipment specified here for the tests should be regarded as recommendations. Equivalent units produced by other manufacturers may be used.

Test equipment	Requirements	Recommended type	Manufacturer	Used in section
Oscillo-scope	With probe 10:1	475	Tektronix	7.3
Signal generator	800 Hz to 150 kHz Level constancy $\leq$ 0.05 dB	PS-4	W & G	9.3
	800 Hz to 150 kHz Intrinsic frequency response $\leq$ 0.05 dB	PS-8	W & G	9.4
	300 Hz to 200 kHz	TFPS-75 or PS-3	W & G	7.2.1, 9.1
	20 Hz to 200 kHz	PSE-11	W & G	7.2.1

Test equipment	Requirements	Recommended type	Manufacturer	Used in section
Level meter	20 Hz to 200 kHz	SPM-11	W & G	7.2.1
	6 kHz to 620 kHz	SPM-6	W & G	7.2.1
Calibrated level meter	10 Hz to 300 MHz	EPM-1	W & G	9.4
Unbalanced measuring probe	75 ohm, BN 572/0	TK-10		
Balanced measuring probe	75 ohm, BN 668	TKS-10		
Measuring probe adapter	150 ohm, BN 668/11	TKS-150		
T-branch	75 ohm, BN 595/1	---		
Digital probe	Display of H or L state and of the duty cycle	TKL-5 or TKL-12	W & G	7.3, 7.4, 7.5, 7.6, 7.7
Adapter board	Extension of internal connections	BN 618/19	W & G	7.1, testing of boards while the unit is switched o

Table 6-1 Test equipment used

6.5 Ordering spare parts

The most important specifications for required spare parts can be found in the parts lists. Components with Bv. or WN numbers are to be ordered in the factory. In addition to the order no. (BN), the unit serial number -

this is located on the underside of the left handle - must be specified, together with the type and identification letter for complete plug-in boards or the position number for discreet components.

Example 1:
Ordering a plug-in board:

BN 618/No. 15372 B/618-G

In this case, BN 618 is the order number of the unit PMD-a, 15372 is the unit serial number, B is the unit series, 618-G is the plug-in board "control".

Example 2:
Ordering a filter:

BN 618/No. 18251 C/618/13

In this case, Bn 618 identifies the unit PMD-1, 18251 is the serial number, C is the unit series, 618/13 is the filter "CCITT psophometric and low-pass 3.5 kHz".

Example 3:
Ordering a transistor for a circuit in the unit:

BN 618/No. 18463 C/T 103

T 103 in this case identifies a transistor in the power supply unit of the PMD-1.

6.6 Abbreviations and symbols

To provide a clearer view in text and circuit diagrams, the following abbreviations and symbols are used:

Battery	B	
Connector/Plug	Bu/St	
Diode, rectifier	Gl	
Zener diode	Gl	
Thyristor	Gl	
Voltage controlled capacitor	(Varicap)	
Inductance	L	
Meter	J	
Capacitor	C	
Resistor	R	
Negative temperature coefficient resistor	R	
Potentiometer	P	
Crystal	Q	
Relay	Rel	
Relay contact	rel	
Switch	S	
Fuse	Si	
Indicator lamp	SL	
Transistor	T	
Unijunction, FET T	T	
Transformer	Ü	

6.7 Colour code

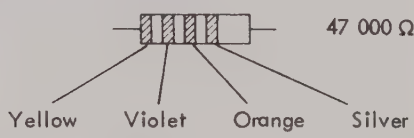
Color code for resistors and capacitors

Color	First and Second ring	Third ring	Fourth ring	Fifth [1] ring
	First and Second number	number of zeros	Tolerance in %	Voltage rating
Black	0	0	-	-
Brown	1	1	1	100
Red	2	2	2	200
Orange	3	3	3	300
Yellow	4	4	4	400
Green	5	5	5	500
Blue	6	6	6	600
Violet	7	7	7	700
Grey	8	8	8	800
White	9	9	9	900
Gold		x0,1 [2]	5	1000
Silver		x0,01 [2]	10	2000
Colorless			20	500

1) only used for capacitors
2) Multiplier for values under 10

Capacitors are usually marked with a row of colored dots or else rings as with resistors. The row starts at the dot closest to one end of the capacitor.

Resistors are marked usually with rings starting at the head. Usually the body of the resistor is used as the first color point, and as second point a cap. The third point (number of zeros) is a point or ring on the body of the resistor (not used when the ring and the body are the same color. The tolerance is identified by the color of the second cap.



Abbreviations of wire insulation colors

bl	blue	rs	pink
bk	uninsulated	rt	red
br	brown	Schirm	screen
fl	colorless	sw	black
ge	yellow	vio	violet
gn	green	ws	white
gr	grey	wsbl	white blue

7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

7. FAULT FINDING AND REPAIR INSTRUCTIONS

7.1 Functional test of the unit and of the plug-in boards

If the results of the functional test in accordance with Section 5.1 do not agree completely with the specifications, it is recommended to first localize the fault to the digital section or the analog section of the unit.

Correct operation of the digital section is indicated, with continuous measurement (S 805 set to "REPET", S 807, for example, to "1 s") as specified in Table 5.1, by the illuminated symbol "Unit measuring" and by regular extinction of this illuminated symbol.

In order to determine whether the fault, in the case of failure of the measuring cycle is caused by the control, connect point 19 of the control board ⑤ to ground. If the measuring cycle (clock cycle) still does not run, then the fault is located in the digital section; otherwise it is in the analog section.

In the case of faults in the analog section, they will in most cases be located on the plug-in boards attentuator ② and/or converter ③. The aim of fault finding is first to localize the fault to a specific plug-in board or to a functional unit. The following tables, level diagrams, and oscillograms, and the functional description in Chapter 10 are used for this purpose. In the case of faults in the digital section, the signal path should first be followed on the basis of the functional description.

A PMD-1 unit is normally required for functional testing or repair of the plug-in boards. In order to have access to the important points on the plug-in boards, we recommend the use of the adapter board for PMD-1, 2 x 22-

pole. Corresponding solder pins are available on the adapter board for each contact of the socket strip in the unit. The test points in the strip, and thus also certain points within the printed circuit board, are easily accessible at these points.

7.2 Attenuator ②, board 618-K 1

In order to determine whether circuit ② is operating correctly, first test the gain of the attenuator board BN 618-K 1.

7.2.1 Manual level range selection

Settings on the PMD-1:

- Level range switch S 801 to manual
- Measurement initiation switch S 805 to "REPET" (continuous measurement)
- Integration time switch S 807 to "1 s"
- Input impedance switch S 803 to 600 ohm

Test configuration

- Connect signal generator, e.g. PSE-11, PS-3, PS-6 or PS-60 (W & G), to the input of the PMD-1, R_i = 600 ohm
- Connect a receiver, e.g. SPM-11, SPM-3, SPM-6, or SPM-60 (W & G), to Bu 203, $R_I \geqq$ 10 kohm

Check

- Select generator frequency between 20 Hz and 200 kHz. Set up the transmit level within the table values and set level range switch S 802 accordingly.
- Check whether the overall gain is correct in accordance with Table 7-1 and - if there is a deviation - whether the preattenuator and attenuator are set as specified.

Level range	1st preatten-uator 20 dB rel 204/205	2nd preatten-uator 20 dB rel 206/207	1st atten-uator 10 dB T 202	2nd atten-uator 20 dB rel 208	3rd atten-uator 10 dB T 203	Gain of the atten-uator board ② in dB
0...+ 20 dB	x	x	x	x	x	approx. - 50
- 10...+ 10 dB	x	x	x	x		approx. - 40
- 20... 0 dB	x	x	x		x	approx. - 30
- 30...- 10 dB	x	x	x			approx. - 20
- 40...- 20 dB	x		x		x	approx. - 10
- 50...- 30 dB	x		x			approx. 0
- 60...- 40 dB			x		x	approx. + 10
- 70...- 50 dB			x			approx. + 20
- 80...- 60 dB						approx. + 30

x = attenuator connected

Table 7-1

If the measured values deviate from those specified in Table 7-1, we first recommend a level check in the attenuator board ② in accordance with Figure 7-1, followed by possible checking of the relays and of the preceding gate ICs, transistors, etc. If the illuminated symbol "Overload" does not light when the level is too high, the transistors T 205, T 206, and T 207 should be checked for correct function, together with the monoflop IC 204.

Settings on PMD-1:

- Connect signal generator with f = 100 kHz/0 dB to Bu 201 of the PMD-1
- Set S 805 to continuous measurement
- Set S 801 to "automatic" (-10 to + 10 dB)
- Set S 811 to "20 Hz ... 200 kHz"
- Measure the level with high impedance test probe (e.g. W & G TK-12)
- Measure voltages with multimeter 100 kohm/V

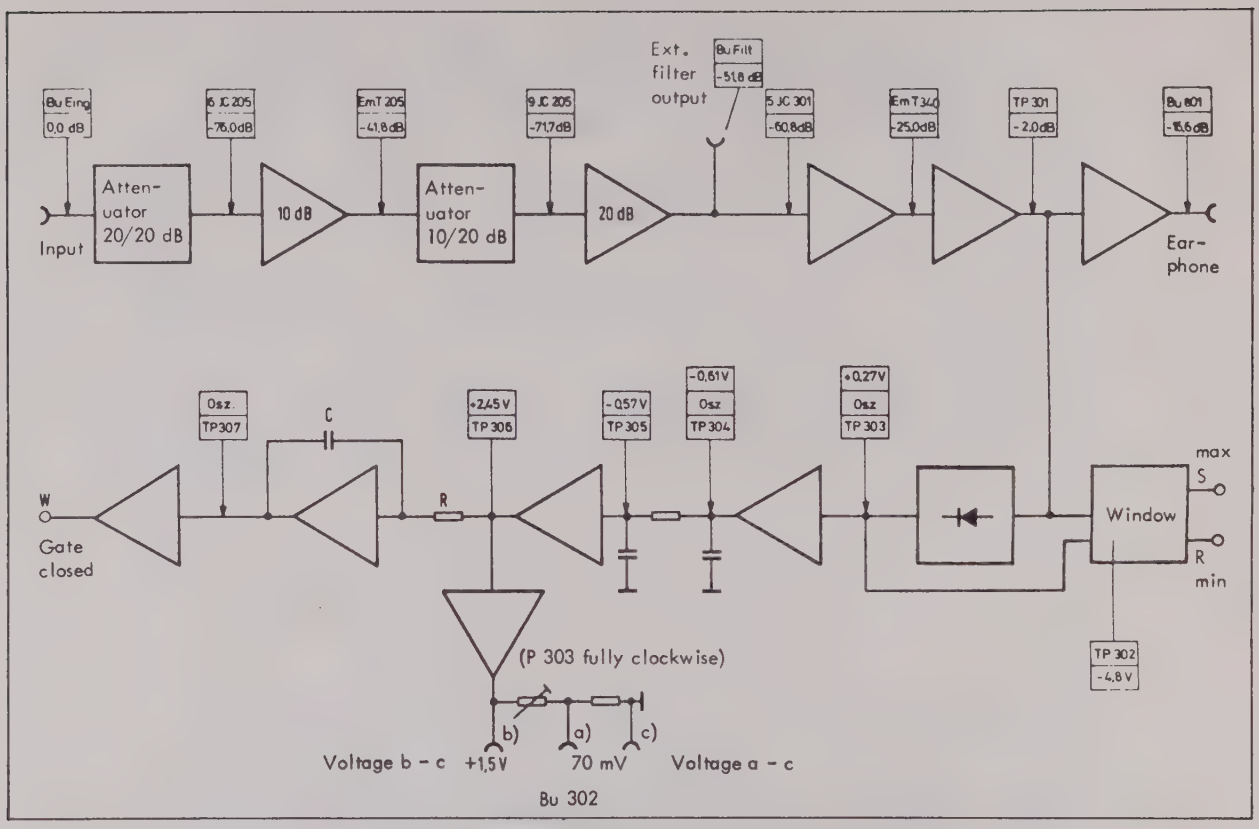


Figure 7-1 Levels and voltages in the attenuator board ② and converter board ③

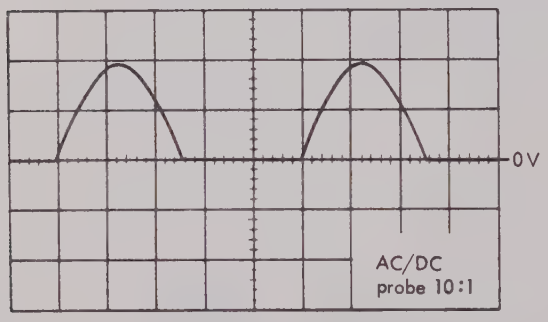


Figure 7-2 TP 303; 0.5 V/cm; 2 us/cm

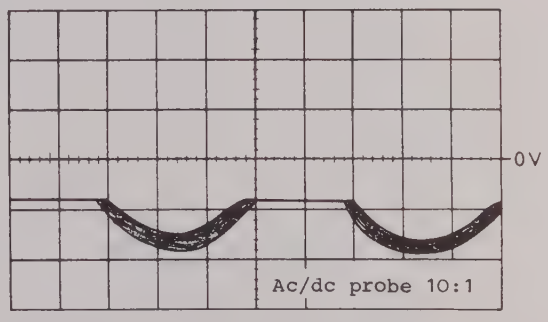


Figure 7-3 TP 304; 0.5 V/cm; 1 us:cm

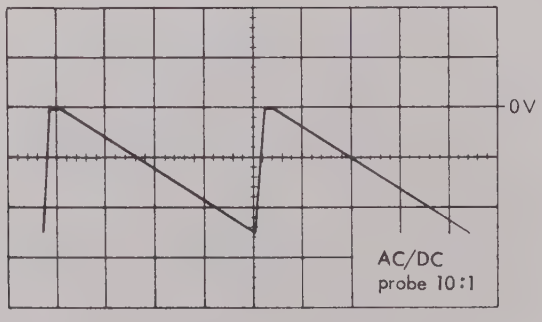


Figure 7-4 TP 307; 1 V/cm; 50 ms/cm

7.3 Converter ③, board 618-J

If the measured values agree with those specified in Table 7-1 and if the unit still does not measure correctly, first check the converter board on the basis of the level diagram for board ③ (Figure 7-1) and the oscillograms (Figure 7-2 to 7-4). The PMD-1 is to be set up in accordance with the specifications in Figure 7-1.

Tables 7-2 and 7-3 provide further hints for fault localization in board ③. In this description, "Idle state" means that a single measurement has been executed and completed.

Settings on PMD-1:

- Connect signal generator with f = 100 kHz/0dB to Bu 201
- Set S 805 to "Single measurement"
- Set S 803 to "600 ohm"
- Set S 811 to "20 Hz ... 200 kHz"

Measure the voltages in accordance with Table 7-2 with a multimeter, 100 kohm/V.

Test point	Voltage
Test point 306	+ 2.45 V
Gate T 324, 325, 326	- 11.7 V
Gate T 330	+ 8 mV
Gate T 330'	- 8 mV
pins 2 + 3, IC 309	+ 1.45 V
pin 1, IC 309	- 630 mV
Test point 307	+ 10 mV
pins 5 + 6, IC 309	+ 10 mV
pin 7, IC 309	- 8 mV
Base T 338	+ 650 mV
Collector T 338	+ 45 mV

Table 7-2 Voltages in converter in idle state

Fault	Probable cause	Functional description and testing of
Automatic attenuator alignment does not work	Window circuit defective	10.4.4.-IC 310, TP 30" Max. switching stage T 315 Min. switching stage T 316 Signals at points S, R
Constant current circuit does not work	L signal "Current on" missing at point V	10.4.5.-Control (5) 7 Discharge FF, IC 512/2.2 Integration FF, IC 507/2.2 Zero MF, IC 510
	T 336, T 337, Gl 318, Gl 319 defective	10.4.5
Analog-digital converter does not work (correctly)	L signal "Release converter" at point U missing	10.4.6.- Control (5) U Integration FF, IC 507/2.2 Zero mF, IC 510
L signal "Gate closed" does not appear at point W Constant current circuit inoperative	IC 309 T 338	10.4.6
The indications "Unit measuring" and overload are continuously lit on the panel	Incorrect operation e.g. when measuring narrow band noise	Do not select automatic level adjustment, set S 801 to manual!

Table 7-3 Fault localization on the converter board (3)

7.4 Attenuator control ④, board 618-H

If the functional checks in 7.3 (attenuator ②) and 7.4 (converter ③) are correct in all points and if the unit still does not measure, the attenuator control ④ should be checked for signal paths and correct functions, (See functional description 10.3).

7.4.1 Manual selection of level range

- Connect signal generator to PMD-1
- Set S 801 to "Manual"
- Vary the generator level as shown in Table 7-3
- Turn S 802 from the range 0 to + 20 dB to - 80 to -60 dB and observe the digital display
- If the digital display does not agree with the generator level, check the counter value IC 408 and/or the digital signals at points N, P, R, 15 with the digital probe, W & G TKL-5 or TLK-12.

Level of input signal (Each range 20 dB)	Points on attenuator control board (4)				Counter value IC 408
	N	P	R	15	
0...+20dB	H	H	H	H	0
-10...+10dB	L	H	H	H	1
-20... 0dB	H	L	H	H	2
-30...-10dB	L	L	H	H	3
-40...-20dB	H	H	L	H	4
-50...-30dB	L	H	L	H	5
-60...-40dB	H	L	L	H	6
-70...-50dB	L	L	L	H	7
-80...-60dB	L	L	L	L	8

Table 7-4

7.4.2 Automatic level range selection

- Set S 801 to "automatic"
- Set S 808...810 (relative level) to 00.0
- Vary the generator level as shown in Table 7-3 and observe the digital display
- If the digital display does not agree with the generator level, test the counter value and/or the digital signals as specified in Section 7.4.1.

Further fault localization:

- Check the digital signals at points 14 and S, see functional description 10.4.4 of converter ③.
- Check the digital modules on board ④, see functional description 10.3 of the attenuator control ④.

7.5 Control ⑤, board 618-G

If the analog section of the PMD-1 in the attenuator ② and converter ③ operates correctly, the digital section must be tested.

As board (5) contains mainly digital modules, first check whether all input and output signals are present and correct. The following list contains the most important signal.

Settings on PMD-1:

- Set S 801 to "Manual"
- Set S 807 to integration time 0.2 s
- Set S 808...810 to relative level 00.0
- Set S 805 to "REPET" (continuous measurement)
- Set S 803 to input impedance 600 ohm
- Set S 811 to wide band "20 Hz...200kHz"

- Connect the signal from the signal generator and test the following signals with the W & G digital probe TKL-5 or TKL-12:

Input signals

Point	Signal designation	Comes from
E	Store feedback	Counter ⑦ E
V	Converter interlock	Attenuator control ④ V
H	Time base	Time base ⑥ H
19	Gate closed	Converter ③ W

Output signals

Point	Signal designation	Goes to
7	Current on	Converter ③ V
		Time base ⑥ 7
		Counter ⑦ 7
U	Release converter	Converter ③ U
9	Zero	Time base ⑥ 9
F	Measuring identification	Counter ⑦ F, Display bus (8) bP and cF

7.6 Time base and logarithm conversion ⑥, board 618-F

On this board, the signals 2.5 MHz (from multivibrator T 601/T 602) and "Current on" at point 7 are particularly important. Otherwise, the comments in Section 7.5 apply, including the settings on PMD-1.

7.7 Counter ⑦, board 618-C

Settings on the PMD-1 as specified in Section 7.5.

Input signals which are important for display of the measured result:

Point	Signal designation	Comes from
12	Relative level	Control ⑤ 10
11	+20 dB range	Attenuator control ④ 11
ZY XW	Attenuator	Attenuator control ④, Z, Y, X, W
F	Measuring identification	Control ⑤ F
9	Zero	Control ⑤ 9
15	Counting pulses from logarithmic converter	Logarithmic converter ⑥ 15

Output signals

Point	Signal designation	Goes to
E	Store feedback	Control ⑤ E
VU TS	$2^0 \times 10^{-1}$ (IC 719/4./4.3.)	Display bus ⑧ c 18/17/16/15
RP NM	$2^0 \times 10^0$ (IC 715/4./4.3.)	Display bus ⑧ c 14/13/12/11
LK JH	$2^0 \times 10^1$ (IC 712/4./4.3.)	Display bus ⑧ c 10/9/8/7

9. ALIGNMENT INSTRUCTIONS

9. ALIGNMENT INSTRUCTIONS

9.1 Basic attenuation of the filters

Alignment of the filter curves in accordance with Sections 3.3.1 to 3.3.6, with respect to their frequency response, would require a complex test configuration and is therefore not possible without further problems. On the other hand, alignment of the basic attenuation can be carried out in a simple manner.

Required test equipment:

1 Signal generator TFPS-75
1 PMD-1, equipped with filter boards

Settings on TFPS-74: R_i = 600 ohm, level approx. 0 dB

Settings on PMD-1:

- R_E (S 803) = 10 kohm
- Set S 805 to "REPET" (continuous measurement)
- Set S 807 to integration time 0.2 s
- Set S 811 to "20 Hz ... 200 kHZ"
- Set up the relative level with S 808...S 810 so that the PMD-1 indicates 00.0 dB
- Set S 801 to the various filters
- Align the basic attenuation with the potentiometers specified in Table 9-1 to the reference frequency so that the PMD-1 indicates 00.0 dB

Filters with weighting	Pot.	BN	Frequency (Hz)	Filters without weighting	Pot.
Psopho-meter	P 1301	618/13	800	Low-pass, 3.5 kHz	P 1305
CCITT sound radio	P 1401	618/14	1000	Band pass filter 31.5 Hz to 20 kHz	P 1402

Filters with weighting	Pot.	BN	Frequency (Hz)	Filters without weighting	Pot.
CCIR sound radio (neutral)	P 1501	618/15	6300	Band pass filter 22 Hz to 20 kHz	P 1502
C weighting filter	P 1601	628/16	1000	3 kHz flat weighting	P 1602
US program weighting	P 1701	618/17	1000	15 kHz flat weighting	P 1702
A weighting filter	P 1801	618/18	1000	Band pass filter 31.5 Hz to 16 kHz	P 1802

9.2 Offset of the converter board ③

Necessary test equipment:

DC coupled oscilloscope for display of the alignment, PMD-1, fully equipped.

- Set S 802 to "+ 20 dB"
- Set S 811 to "Filter external"
- Connect converter board via adapter board

Offset of IC 310

- Adjust P 307 so that there is no voltage at TP 302

Offset of IC 305

- Connect oscilloscope to TP 306
- Short-circuit TP 305 to ground
- Adjust P 308 so that there is no voltage at TP 306.

9.3 Calibration of RMS value/peak value (Zero and maximum value)

Required test equipment:

Signal generator 800 Hz to 150 kHz, error limits of the output level ± 0.05 dB, e.g. W & G PS-4

Settings on PMD-1

- Set S 801 to "Manual"
- Set S 802 to "-20 to 0 dB"

9.3.1 Calibration frequency 10 kHz

- Set the generator output level alternately to -0.1 dB and - 19.9 dB

Calibration of RMS value

- Set S 807 on PMD-1 to "1 s"

a) Adjust P 305 at -0.1 dB so that the connected level is displayed on the PMD-1

b) Adjust P 302 at -19.9 dB so that the connected level is displayed.

Normally, alignment steps a) and b) must be repeated alternately several times.

Calibration of peak value

- Set S 807 on PMD-1 to "2 s"

a) Adjust P 304 at -0.1 dB so that the connected level is displayed on the PMD-1.

b) Adjust P 306 at -19.9 dB so that the connected level is displayed.

Repeat alignment steps a) and b) alternately as required.

9.4 Alignment of frequency response

Test equipment: Signal generator 800 Hz to 150 kHz with intrinsic frequency response of $\leq$ 0.05 dB
or
amplitude control of a lower quality signal generator by means of calibrated level meter EPM-1 by W & G (See Section 3.4.6 in the operating instructions for EPM-1)

Test equipment settings:

Output level -50 dB, f = 800 Hz, R_i = 600 ohm

PMD-1: S 801 to "Manual"
S 802 to "-60...-40 dB"
S 803 to 600 ohm
S 805 to "REPET"
S 807 to "1 s"
S 811 to "20 Hz...200 kHz"

Note the measured value at 800 Hz, increase the signal generator frequency to 180 kHz, and adjust C 213 so that the value noted above is again displayed.

Signal generator level to 0 dB, f = 800 Hz
S 802 to -10...+10 dB.

Note the measured value at 800 Hz, increase the signal generator frequency to 150 kHz, and adjust C 224 so that the value noted above is again displayed.

10. DESCRIPTION OF FUNCTION

10. FUNCTIONAL DESCRIPTION

It is assumed that the reader has already read Chapters 1 to 6 of the operating instructions. The following descriptions provide further details concerning the function of the plug-in boards and of the signal path within the unit. Complete circuit diagram with printed circuit board components can be found in the Appendix.

The PMD-1 consists of the following assemblies, most of the important parts in these assemblies being in the form of plug-in boards:

Power supply unit (1)
Attenuator (2)
Converter (3)
Attenuator control (4)
Control (5)
Time base and logarithm converter (6)
Counter (7)
Remote control board (12)

The following filter boards are available:

Psophometer filter (13)
Sound radio filter CCITT (14)
Sound radio filter CCIR (15)
C weighting filter (16)
US radio filter (17)
A weighting filter (18)

10.1 Power supply unit (1)

The power supply supplies the following dc voltages:

+ 250 V $\pm$ 10 %, + 20 V (unstabilized)
+ 15 V, - 15 V, + 5 V (electronicallystabilized)

The regulation circuits (marked with "U_{const}" in the circuit diagram) are constructed around a type L 123 TL integrated circuit which is connected in the normal manner.

10.2 Attenuator ②, board 618-K 1

The attenuator circuit has the following tasks:

a) It provides the input impedances 600 ohm or 10 kohm for balance and 100 kohm for unbalanced measurements with the aid of relay circuits - controlled by the pushbutton switch S 803.

b) It converts all measured voltages in the range between -80 and +20 dB in such a manner that they lie in the 20 dB working range of the converter.

   In the position "Manual" of the level range switch S 801, this is achieved by the gates connected to the level range switch S 802, which switch on relays and switching transistors in circuit ②, thus connecting or removing various attenuator stages or combining such stages.

In the position "Automatic" of S 801, signals from the attenuator control ④ and the converter ③ connect or disconnect various attenuators in circuit (2).

c) The attenuator circuit ② also monitors for short or continuous overloads and generates a signal with the aid of the overload monoflop for display by means of an illuminated signal.

10.3 Attenuator control ④, board 618-H

This circuit controls the function of the attenuators on board ② as a function of the position of the range counter IC 408, which is the heart of the attenuator control circuit. In the case of manual setting up of the level range with switch S 802, the position of this switch

generates digital signals which are passed to the counter via points 19, 20, 21 22. In the case of automatic selection of the level range, the attenuator functions are controlled as follows:

IC 408 starts counting with a value of 0 which corresponds to the least sensitive level range of the PMD-1. If the level to be measured lies within the selected range, then H signals are present at board pins 14 (minimum level) and S (maximum level). This means that there is also an H signal at board pin L or at pin 4 of IC 408; this prevents the attenuator setting from being changed.

If the level to be measured lies below the selected measuring range, then the "window circuit" on converter board ③ supplies an L signal at pin ④ 14. As coincidence is no longer fulfilled at IC 414/2.2 and IC 418, diode G1 401 cuts off. This means that the clock multivibrator (IC 401) starts to oscillate with a cycle length of approx. 65 ms. The output pulses of this multivibrator are fed via C 402 to the clock monoflop IC 402 which in turn increments the range counter IC 408 and simultaneously starts the interlock MF 1 (IC 403). The output pulse of this MF is fed to the control ⑤ via pins ④ V and ⑤ V.

The signal "inhibit converter" prevents release of the conversion cycle before the rectifier of circuit (3) has settled.

The range counter continues to count until either the L signal at pin ④ 14 disappears or until the counter reaches the value of 8. This corresponds to the most sensitive position of the level range switch. The counter signal "8" then switches off the clock multi-vibrator via the NAND gate IC 417/4.1 and via IC 418.

The setting of the attenuator is not changed during conversion and zeroing. In the remaining time, the measured signal can vary at will, the attenuator being set appropriately. For this purpose, the max.-min. flip-flop IC

417/4.3 and /4.4 determines the direction of counting $V/\overline{R}$ (forwards/backwards).

If the level of the measured signal changes very rapidly, then the min. and max. monoflops IC 415/2.1 and IC 415/2.2 insure that an interval of approx. half a second is maintained for the change of range in order to prevent undue wear on the relay contacts.

10.4 Converter ③, board 628-J

The converter board ③ contains the following functional units:

Selection circuit for the filters
Output amplifier and low-pass filter
Rectifier and weighting circuit
"Window circuit"
Constant current circuit
Analog-digital converter

10.4.1 Selection of the filters

One of the filter outputs 1a, 1b, 2a, 2b at board pins 6,5,8,7 or the external filter via Bu 301/a is selected by means of the selection lines at one of the board pins 10...14. An L signal, coming from S 811 or from the remote control board (12), causes one of the transistors T 307...T 310 or T312 to conduct, together with the appropriate FED transistor. R 301...R 304 are defined load resistors for the filters. The voltage divider R 305/R 308 attenuates the signal coming from attenuator (2) 16 by 9 dB in the position "20 Hz to 200 kHz" (wide band) of the weighting switch S 811, this attenuation corresponding to the basic attenuation of the filter. The input Bu 301 "filter external" is loaded with approx. 600 ohm by R 307 and R 306 ‖ P 301. P 301 permits basic attenuation equalization of the external filter with a range of approx. 3 dB.

10.4.2 Output amplifier and low-pass filter

The amplifier IC 301/2.1 operates in non-inverting mode; T 340 carries the load current. The antiparallel diodes prevent overloads.

For RMS value measurement, the voltage divider R 323/R 322 determines the gain. In the case of peak value measurements, FET T 341 connects resistor R 3141 parallel to R 323, thus reducing the gain by approx. 15 dB.

The following low-pass filter with L 302 and C 331...C 333 becomes affective at frequencies above 220 kHz; it attenuates noise voltages which, at frequencies below 1.5 MHz, could cause measuring errors in the most sensitive range.

The emitter follower T 313 permits simultaneous driving of the rectifier via R 336, of the weighting circuit via R 359, of the earphone amplifier via R 334, of the overload circuit via Gl 301, and of the window circuit via R 340. The earphone isolating amplifier IC 303/2.1 reduces the level by approx. 3 dB. In the case of automatic range selection, the level at the earphone socket is always between -10 and 0 dB (without load!); in the manually selected fixed ranges, the level lies between -15 and +5 dB.

In the case of peak value measurement, T 342 disconnects resistor R 3143 so that the gain of isolating stage IC 303/2.1 is then +12 dB.

The overload circuit (T 339, T 314) monitors the level ($\leqq$8 dB) at test point TP 301. T 339 cuts off if the voltage at TP 301 becomes more negative than - 8 V. In this case, T 314 conducts and activates the signal "rectifier overloaded"; this triggers the overload monoflop in the attenuator circuit via ③ J and ② 10. The "overload" symbol on the display panel lights as long as this monoflop is active.

10.4.3 Rectifier and weighting circuit

The level present at TP 301 is connected via R 336 to the inverting input of IC 302/2.1. The negative half cycles are phase-shifted by 180°. The negative feedback loop is connected via Gl 305 and resistor 338. As R 336 and R 338 are exactly equal, the amplitude of the voltages at test points TP 301 and TP 303 is also exactly equal. Only the positive half cycles are available at TP 303 (See Figure 10-1).

Figure 10-1 (see page 10-7)

A rectified voltage is generated from the voltages at test points TP 301 and TP 303 by current addition in resistors R 358 and R 359. These resistors have a ratio of 1:2. This means that the voltage from TP 303 is amplified by a factor of 2 by IC 303/2.2 and the voltage at TP 301 by a factor of only 1. Figure 10-1 shows how the currents are added at the sum point, pin 8 of IC 302/2.2, at any given time. During the first half cycle, a positive current flows only through R 359.

The next half cycle through this resistor is negative. At the same time, a positive current with twice the value flows through R 358. This means that a positive current with the same value as in the first half cycle again flows through the summing point. Although the circuit at TP 303 provides only half-wave rectification, the complete circuit operates as a full-wave rectifier.

The weighting circuit has the task, for RMS value measurement, to modify the rectified peak voltages in such a manner that the PMD-1 displays the pseudo-RMS value. Figure 10-2 shows the principle of the weighting circuit for RMS value measurement.

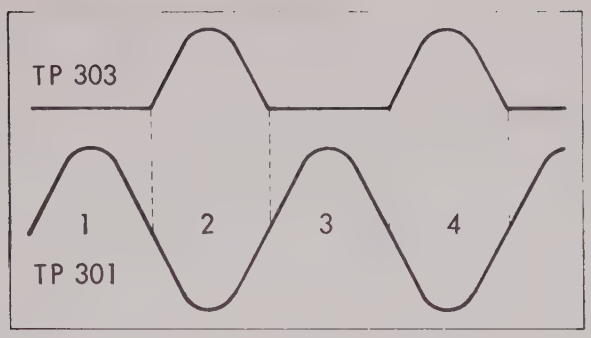


Figure 10-1

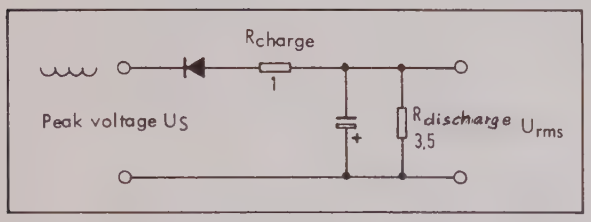


Figure 10-2

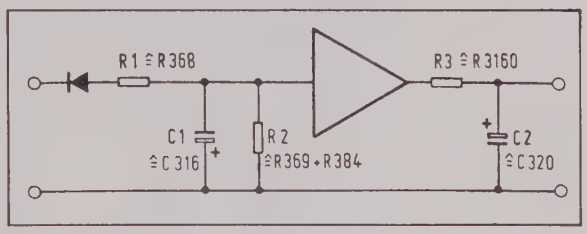


Figure 10-3

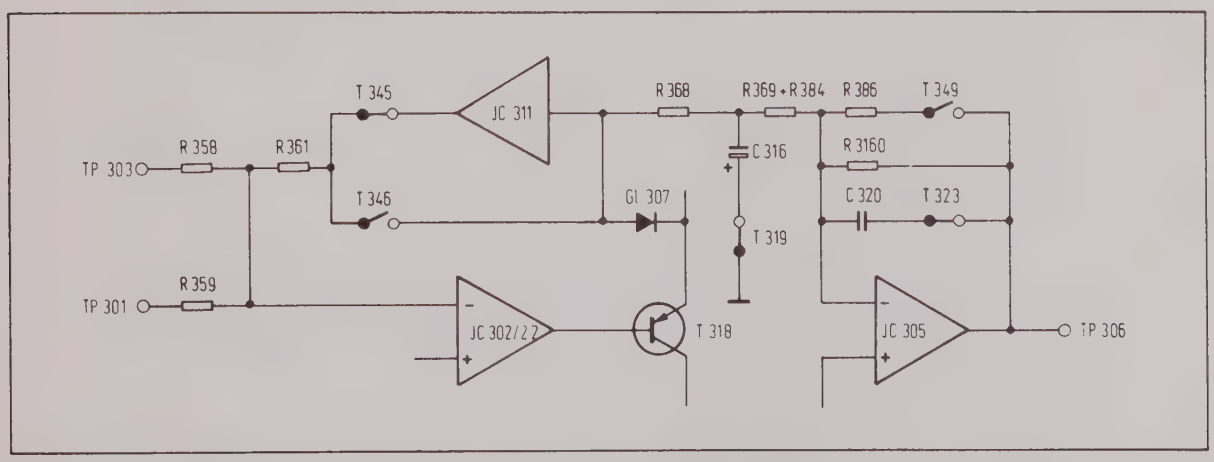


Figure 10-4 Partial functions of the weighting circuit for peak value measurement

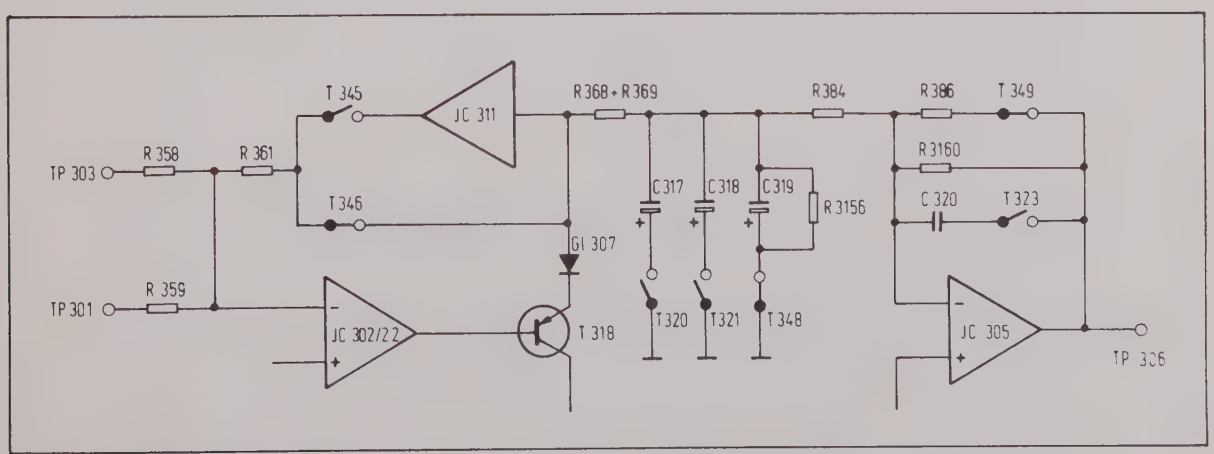


Figure 10-5 Partial functions of the weighting circuit for RMS value measurement

The charging resistance is implemented in the circuit by resistors R 368 and R 369. Depending on the measuring time, one of the capacitors C 317 or C 318 and C 319 is connected as the charging capacitor. The discharge resistance results from series connection of R 361, R 368, R 369 and parallel resistors R 3156, R 384.

The principle of peak value measurement is shown in Figure 10-3. This measuring mode requires the following time constants:

R1 . C1 = 1 ms	for charging
R2 . C1 = 300 ms	for discharging
R3 . C2 = 130 ms	for charging and discharging (Meter time constant)

Switching of the weighting circuit between peak value and RMS value measurement requires a large number of separate switching functions. Figures 10-4 and 10-5 show these in a simplified form.

A current is fed into the plus input of the amplifier via P 302 and R 363 (additionally from P 306 via T 344 and R 3149 for peak value measurement) for compensation of the offset of IC 302/2.2.

A dc voltage which corresponds to the input level is present at TP 306. This analog voltage is passed to the analog-digital converter and, via the isolating amplifier IC 303/2.2, to socket Bu 302.

At this point, 150 mV $\pm$ 30 mV into 100 ohm is present between a and c (ground), e.g. for a recorder; between b and ground there is a voltage of approx. 5 V into 5 kohm, e.g. for display units. The recorder voltage can be adjusted with P 303 on the rear of the unit.

Note: 150 mV/5 V are available at Bu 302 only for "full scale deflection".

10.4.4 "Window circuit"

For automatic attenuator adjustment, the automatic attenuator control of the PMD-1 requires control signals which cause the currently selected level range to be switched to a more suitable range if it is too large or too small. The window circuit is used for this purpose.

IC 310 with G1 302, G1 303 generates an analog dc voltage from the voltages at TP 301 and TP 303. This voltage affects the thresholds of the maximum-minimum switching stages T 315, T 316.

If the voltage at TP 302 becomes more negative than -8.5 V, then T 315 cuts off, resulting in a L signal at pin ③ S ("max. level"). This is fed to the max. MF of the attenuator control ④.

For the minimum switching stage, which operates in a similar manner, the critical value of the voltage is -2.5 V. The threshold voltages (more negative than -8.5 V or - 2.5 V) are present at TP 302 as soon as the connected level is less than approx. 5 dB from the end of the range.

As the window circuit has to be effective for both RMS and peak value measurements, T 343 disconnects resistor R 3145 for peak values, thus increasing the gain of IC 310 by 15 dB. Adjustment of the offset voltage, which is particularly important at this point, is carried out with P 307.

10.4.5 Constant current circuit

A constant current circuit is required for the functional unit "analog-digital converter" on board ③. This circuit is switched on by the L signal "current on" from the control ⑤ 7 vy ③ V. T 336 switches on and G1 318 conducts. The voltage at the Zener diode G1 319 is now also

present at the emitter of T 337. As this voltage is constant, a constant emitter and collector current flows. The constant current is switched off by switching the signal "current on" to 5 V, thus switching off T 336.

As a result of this, Fl 318 cuts off and the base potential of T 337 switches to - 15 V. No further current can flow.

10.4.6 Analog-digital converter

Converters of this type use the dual slope principle. In such converters, a capacitor is charged via a resistor from the voltage being measured during the integration time T_i and is then discharged with a constant current during the measuring period T_M. The time required for discharge is then a dimension for the connected voltage.

Figure 10-6 Principle of the dual slop method (Output voltage U_A) (see page 10-11)

The dependency of the measuring time T_M on the value of the voltage being measured U_M is shown in Figure 10-6, together with the basic diagram. As the converter in the circuit ③ uses a modified dual slope method, its basic circuit is also modified. Figure 10-7 shows the principle of peak value measurement, Figure 10-8 the principle of RMS value measurement, both in a slightly simplified form.

Function for peak value measurement

During the interval (neither display nor discharge time), transistor T 331, T 322, T335 conduct. The so-called drift equalization is carried out. For this purpose, the input is connected to ground via T 322 and T 331.

The output voltage U_A is fed back to the positive input via T 335 and capacitor C 322 is simultaneously charged. This means that a exactly O V is present at the output of IC 309/2.1.

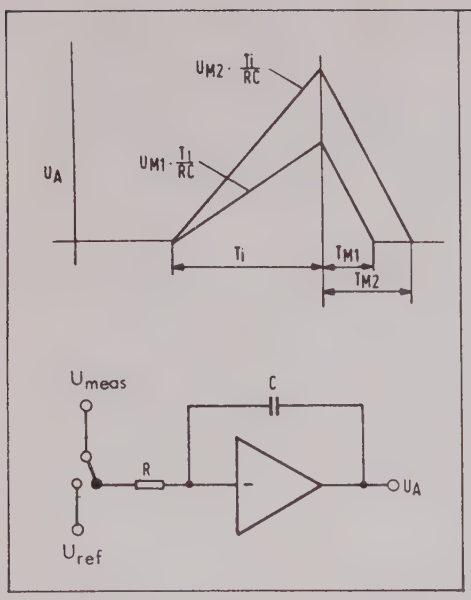


Figure 10-6 Principle of the dual slope method (Output voltage U_A)

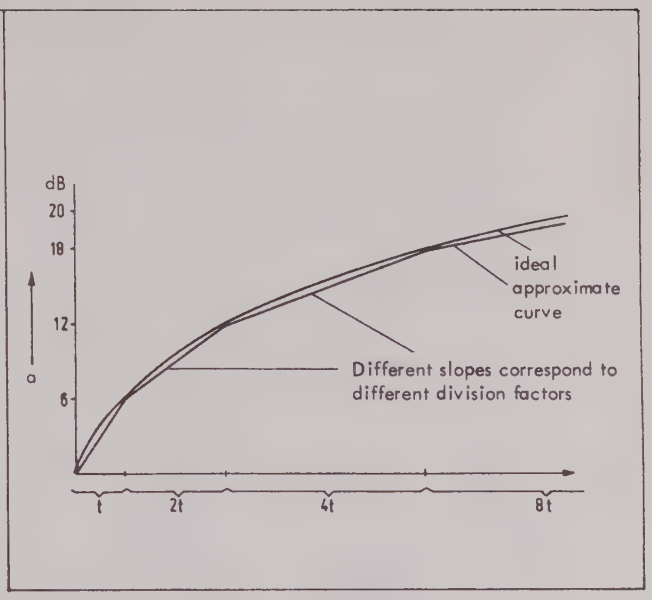


Figure 10-9

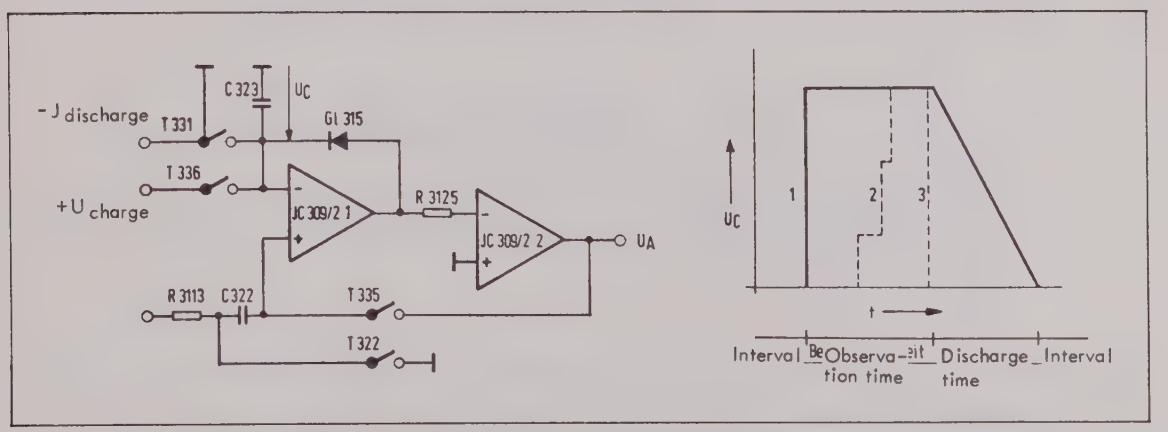


Figure 10-7 Principle of the modified dual slope method for peak value measurement (Charge voltage U_C)

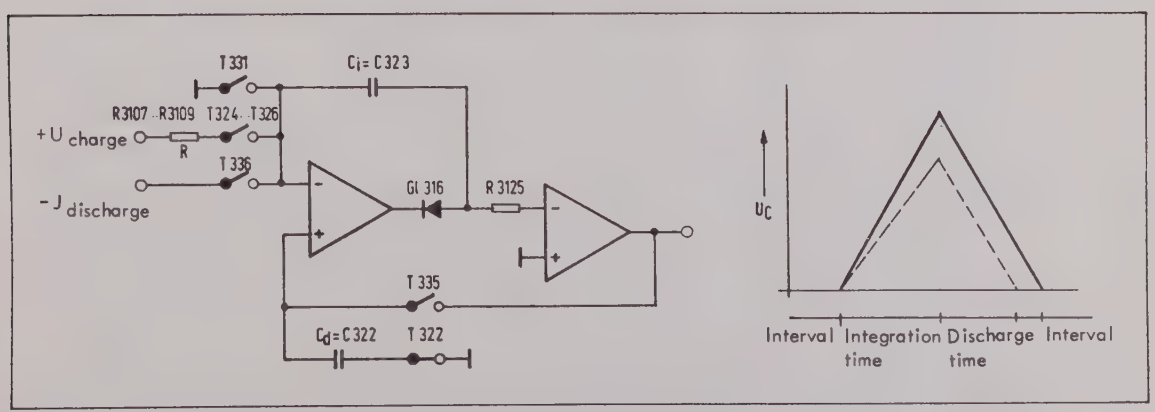


Figure 10-8 Principle of the modified dual slope method for RMS value measurement (Charge voltage U_C)

In the subsequent observation time, the transistors T 331, T 322, and T 335 are again cut off. The drift storage capacitor C 322 is connected in series with the voltage to be measured and holds its charge for a period of more than 10 s.

The peak value storage capacitor C 323 is charged via GL 315 to the maximum peak value which exists during the observation time. Lower voltages after this maximum value cannot discharge C 323 as this is prevented by Fl 315. After the observation time has been completed, the L signal "current on" arrives from the control ⑤ 7. Transistor T 336 switches on the constant current and T 322 again conducts. As soon as C 323 has been completely discharged, the comparator IC 309/2.2 generates a signal to the control. The constant current is now switched off and the interval status is again established.

The discharge time of C 323 is the dimension for the voltage to be measured. During this time, a logarithmic clock pulse is counted into the main counter ⑦. The result of measurement is now displayed and the measuring cycle is complete.

The diagrams for U_C in Figure 10-7 all lead to the same measured result. In the case of diagram 1, there is either a constant level at the input or a maximum peak is reached at the start of the observation time. The shape of curve 2 results from 3 sequential peaks. The largest peak value remains stored and would affect the display and the discharge time. Curve 3 shows that a single pulse just before the end of the observation time would bring the same result as a constant level during the whole period. The typical behavior for peak value measurement is thus displayed. It should be noted that the PMD-1 measures only the pseudo peak value. This means that the RMS value, i.e. 3 dB lower than the peak value, is displayed if a sine wave signal is connected.

Function for RMS value measurement

During the interval, transistors T 331 and T 335 conduct. T 322 always conducts for RMS value measurement. As already described for Figure 10-7, drift equalization is carried out. This insures that the integration capacitor C_i is completely discharged. One of the transistors T 324 ... T 326 conducts with the signal "release converter"; T 331 and T 335 cut off. The integrator is now connected to the voltage to be measured (TP 306) via resistor "R". The integrator charges the integration capacitor C_i via "R". This operation is terminated as soon as the integration time of 0.2, 1 or 5 s is complete. T 324 (... T 326) cuts off. T 336 switches on the constant current. This discharges the integration capacitor C_i until the comparator indicates complete discharge of C_i with a signal. As already described, the discharge time is the dimension for the voltage to be measured.

10.5 Control ⑤, board 618-G

The plug-in board ⑤ contains the functional units

Control circuit
Relative level circuit
Zero

10.5.1 Control circuit

For single measurements, the PMD-1 is released via pin ⑤ 5 and the release FF IC 507/2.1 is set via DG 502. Output 5 of this IC switches to H level. The signal "measuring identification" is now present at pin ⑤ F. When this signal is activated, the zero MF IC 510 is triggered. Only in the case of automatic attenuator adjustment and with the attenuator set to the incorrect range, is this carried out after the signal "inhibit converter" is deactivated, this signal coming from attenuator control ④ V via ⑤ V. During the active

period of the reset monoflop IC 510, a zero pulse is available at board pin 9. This causes the reference level counter (8) IC 815, 517, 518 to be set to the value set up on the reference level switches S 808...S 810. With the trailing edge, the integration flip-flop IC 507/2.2 changes state. In addition, the time base on board (6) is released by the signal "Zero". As soon as the time base signal appears at pin (5) H, the integration FF returns to its idle state. This sets the discharge FF IC 512/2.2. The integration capacitor on the converter board (3) is now discharged with a constant current. When this is complete, then the converter generates the signal "gate closed" at pin (3) W. This resets the discharge FF via pin (5) 19. Resetting of the FF causes the weight time MF IC 50§/2.1 to be triggered via gate IC 504/4.3. This MF is triggered in a different manner if the voltage to be measured is insufficient. In this case, the "gate closed" signal at pin (5) 19 holds the discharge FF IC 512/2.2 in its idle state. Only the "gate closed" MF IC 509/2.2 can be triggered by the integration FF in this case. As the gate IC 504/4.3 is open, due to the idle state of IC 512/2.2, the pulse of the "gate closed" MF can trigger the weight time MF IC 509/2.1. The reference level circuit is active during the active time of this MF.

10.5.2 Reference level circuit

At the start of the weight time, the reference level FF IC 512/2.1 is set. If the reference level is not zero, then the And condition of IC 506/3.3 is fulfilled. H level is present at input 9 of the reference level MF IC 502/2.2 before input 10 switches to H. The RC circuit R 526/523 equalizes the propagation times of IC 506/3.3 and IC 512/2.1. The counter gate IC 511/3.3 and the gate FF IC 513 are now prepared for counting. The next pulse coming from the 2.5 MHz generator (6) sets the gate FF. From now on, the counting gate is open. All further pulses are counted into the reference level counter IC

518, 517, 515. In addition, they are extracted after the counting gate and fed to the main counter ⑦.

The reference level counter counts downwards. As soon as it reaches the value 000, the counting gate is closed via IC 506/3.3, the gate FF is reset, and the reference level MF IC 502/2.2 is triggered. This MF resets the release FF 507/2.1 and the reference level FF IC 512/2.1, and extends the measuring identification signal by its active period. The contents of the main counter are moved to the main store by the L - H edge of the measuring identification signal, thus being displayed. Measurement is now complete.

The gate FF IC 513 prevents distorted pulses from passing through the counting gate, these pulses being capable of incrementing the reference level counter but not the main counter.

When the reference level switches S 808...S 810 are set to 000, or if H signal is present at pin ⑤ 20 (reference level "on"), the reference level MF IC 502/2.2 is triggered immediately at the start of the weight period. In the case of continuous measurement, pin (5) 6 has L level. After each measurement, the release FF IC 507/2.1 is again set for the subsequent measurement by the trailing edge of the storage pulse at pin ⑤ E. The RC circuit R 522/C 520 insures that the continuous measurement starts correctly when the unit is switched on.

10.5.3 Zeroing when switching on

After the unit is switched on, transistor T 501 conducts for approx. 200 ms. This time is determined by C 518 and R 518 + R 519. All flip-flops are set to their idle state. The release FF is released with the trailing edge of the reset pulse and is triggered - with a delay of approx. 500 ns via R 522, C 520 in the case of continuous measurement.

The abort MF IC 502/2.1 has the task of aborting the measurement if the signal "continuous measurement" switches from L to H. The abort MF is triggered via DG 501 but only if the signal "store feedback" has H level. This resets all flip-flops and counters in the unit.

10.6 Time base and logarithm converter ⑥, board 618-F

The board ⑥ contains the functional units

Time base
Logarithm converter
2.5 MHz multivibrator

10.6.1 Time base

The signals at board pins J, K, L determine the dividing factor or the time base by various combinations of L and H signals (See Table 10-1).

IC 608 divides by 5, with one exception. Only in the case of an observation time of 10 s is the division factor switched to 10 by means of IC 607.

Board pin			Time base on
J	K	L	Pin ⑥ H x
H	H	H	0,2 s
H	L	H	1 s
L	H	H	5 s
H	H	L	2 s
H	L	L	5 s
L	H	L	10 s

Table 10-1

x means that pin (6) H changes from H state to L state after the specified times have elapsed - counted from the end of the zero pulse.

10.6.2 Logarithm converter

The logarithmic display is basically achieved by means of a divider chain whose division factor depends on the range of the approximate logarithmic function currently being used (See Figure 10-9).

In addition to the 2:1 division as a coarse approximation, the 6 dB ranges are again divided into four in the PMD-1. IC 620 divides the measuring range into four 6 dB ranges (1:1 and division factors 2, 4, 8). IC 615, IC 609, and IC 604 again divide each 6 dB range into four sections with the division factors 126, 150, 179, 212. This means that the complete measuring range is divided into 16 stages of 1.5 dB each.

The logarithm conversion operation is carried out as follows:

At the start of a measurement, the reset pulse resets all flip-flops to their idle state. 126 is stored in the divider chain. The signal "current on" allows pulses to flow into the divider. The dividers consist of four decrementing SN 74 190 N modules. A pulse is generated at pins 12 and 13 of IC 615 with the 126th clock pulse. The first divider (IC 604, 609, 615) is now again set to 126 with the signal from pin 13 and the pulse from pin 12 is passed on to the following divider IC 620.

This counter was set to 1. Due to the input pulse, it is set to 0. The resulting pulse at pin 13 sets the counter back to 1 and the pulse from pin 12 switches counter IC 619 to 1. The whole operation starts again from the beginning.

After the 15th cycle (= 1.5 dB), the AND condition of IC 618/2.1 is fulfilled. The H-L edge sets IC 619 to 0 by DG 601 and also sets IC 613 to 1. This causes the code converter IC 611/2.1 to apply the new information (divi-

sion factor) to the divider chain. This information is, however, not yet entered.

After a further 126 clock pulse, IC 619 is set to 1. In addition, the new information 150 is now entered in the chain. The following 15 cycles are executed with this new division factor. After the 15th cycle, IC 619 is set to 0 and IC 613 to 2. This means that the new information 179 is presented to the divider chain. Again, it is entered into the chain only with the 15th cycle.

After a further 15 cycles, 212 is entered into the chain. Division is carried out with 212 until IC 613 has a value of 4 and the following output pulse from the divider chain sets the flip-flop IC 624 which is prepared by this value. Setting of this flip-flop causes the following actions: IC 613 is set to 0 via DG 602. The Q output of the FF opens the gate for the counter pulses IC 625/4.1. From now on, the pulses from the logarithm converter are passed via ⑥ 15, ⑦ 15 to the main counter. The reason for this is the following:

The smallest measured value is 0.0 dB. However, the converter operates with voltages of approximately 0 - 10 V. As 0.0 dB corresponds approximately to 1 V and as the time for counting from 0 V to 0.0 dB is equal to the distance from 0.0 dB to 6.0 dB, couting from 0 dB to 6 dB is first carried out, but these counting pulses are not evaluated. After this period, IC 613 is set to 0 and the actual counting operation begins. The following first counter pulse (= 0.1 dB) is still obtained with the division factor 212. This provides a zero shift and a parallel shift of the complete approximate logarithmic function. This error is compensated by calibration of the converter. Further operations then correspond to the 6 dB range already described. When the 20.0 dB value is exceeded, a signal is generated at board pin 13, but only in the period where the main counter has the value 201.

10.6.3 2.5 MHz multivibrator

The 2.5 MHz multivibrator provides the time base, the logarithm converter, and the reference level circuit with pulses. The multivibrator is adjustd to 2.5 MHz with P 601.

The time constant results from the parallel connection of R 626/R 627, potentiometer P 601 and capacitor C 625. Due to the relatively high frequency, the switching times of the two transistors have a considerable effect on the cycle length.

10.7 Main counter (7), board 618-E

The following functional units are located on the counter board:

Main counter	With forwards/backwards control; this accepts counting pulses from the logarithm converter, taking into account the reference level and the polarity.
Main store	This accepts the counter contents from the main counter.
Logical connections for the printer	Initiates release, printing, print identification, and possible red printing.

10.7.1 Main counter

At the start of a measurement, after the attenuator has been aligned, the zero pulse sets the main counter to a value corresponding to that of the attenuators. During the discharge period, counter pulses arrive at the counter from the logarithmic converter. The direction of counting is determined by the signals at board pins 6 (test point), 11 (+20 dB range), 12 (reference level polarity), as shown in Table 10-2.

Board pin				Direction of counting
12	11	6	9	
H	H	L	⎍	downwards
L	H	L	⎍	upwards
H	L	L	⎍	upwards
L	L	L	⎍	downwards
L	X	H		downwards
H	X	H		downwards

Table 10-2

Pin 6 normally has L signal. If the counter overruns (more than 999 upwards or 000 downwards) this point switches to H.

During the weight period (active period of the weight time MF IC 509/2.1), reference level pulses arrive at the main counter from the control board. These pulses are added to or subtracted from the measured level depending on the polarities of the reference level and measured level.

10.7.2 Main store

The counter contents are now transfered to the main store. The store MF IC 722/2.1 provides the pulse for this

purpose. The MF is triggered by removal of the signal "measuring identification", and pin 10 of the MF switches to H, causes IC 711/2.1 to be set and triggering the MF. IC 711/2.1 is reset with the trailing edge of the store pulse and - in the case of continuous measurement - a new measuring cycle is started.

10.7.3 Logical connections for the printer

The store outputs to the printer can be switched to positive logic. The simplest method of executing this change between positive and negative logic is to use exclusive OR gates 7486. If the control input at pin ⑦ 35 switches to H, then the connected signal is inverted; if the signal at pin ⑦ 35 is L, the signal remains unchanged.

During conversion, there must be no overload. Even short term overloads which falsify the measured result set an FF (IC 702/4.2/4.3). The status at this FF is transfered to IC 704 with the store pulse and causes the red ribbon to be selected if this measurement is to be recorded. This signal can be reset only after completion of the following measurement.

IC 706 provides signals for the display indicating whether the measured signal lies above or below the selected measuring range. The "200 signal" (pin ⑦ 13) sets IC 706/2.1 as soon as the logarithm converter emits more than 200 pulses, which corresponds to "above the measuring range". IC 706/2.2 is set via pin ⑦ 7 during the signal "current on" if at least one pulse is passed from the logarithm converter to the main counter. If this one pulse does not arrive, this means that the measured voltage lies below the measuring range.

The two states "above" and "below" are stored in IC 704 and are reset only after completion of the next correct measurement. This storage function causes the arrows ↓ or ↑

to continue flashing after a single measurement outside the range although the correct level has been connected in the meantime.

10.8 Display circuit (8), board 618-B, 618-C, Display and controls

The display circuit contains, in addition to the display and controls, the following special features:

The two flip-flops for start and measurement (IC 807) are constructed so that the output of a gate with high signal is pulled to ground when switches S 804 and S 805 are operated.

IC 812 signals the end of a measurement in continuous measuring mode. This monoflop extends the short time between the measuring cycles to such a degree that it is clearly visible that the illuminated symbol "unit measuring" has been extinguished.

A generator with the frequency of approx. 1 Hz interrupts the signals "below" or "above". The time determining element R 822/C 812 is connected between the input and output of IC 803/4.4.

10.9 Remote control (12), board 618-N or connection board 618-M

The board 618-N permits, together with the output store BN 532/15, remote control of the PMD-1 by means of the program control and evaluation unit PRA-30, with the aid of perforated tapes. All functions - except for the reference level - can be remotely controlled. A large number of the control signals (manual and remote control) are looped through the remote control board. The PMD-1 can therefore measure only when this board is fitted or if it is replaced by the connection board 618-L.

The signal "remote control on" switches the IC's 1201 ... 1204 to remote control mode. This means, for the decoder 74156, that the signals present at pins 1, 2, 3 of the amphenol socket Bu 1201 determine which weighting is selected. These short-circuit proof outputs are connected directly to S 811 on the display board (8).

The multiplex modules SN 74157 N switch between the remotely controlled and manual signals. The suppression circuits DG 1...DG 4 suppress any interference pulses on the cable from the PRa-30 to the PMD-1.

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